

MINISTRY OF EDUCATION AND SCIENCE OF THE REPUBLIC OF ARMENIA

STATE ENGINEERING UNIVERSITY OF ARMENIA

CONFIRMED BY

EXECUTIVE DIRECTOR OF

“SYNOPSIS ARMENIA” CJSC SG

H. MUSAYELYAN

“ \_\_\_ ” \_\_\_\_\_ 2005

CONFIRMED BY

VICE RECTOR OF STATE ENGINEERING

UNIVERSITY OF ARMENIA

R. AGHGASHYAN

“ \_\_\_ ” \_\_\_\_\_ 2005

## **VLSI DESIGN ALGORITHMS**

COURSE PROGRAM

INDEX:

**22.04**

SPECIALIZATION **“ELECTRONIC DESIGN AUTOMATION”**

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The program has been discussed and approved by:

- At the sitting of the SEUA interdepartmental Chair of “**Microelectronic Circuits and Systems**” acting on the basis of “SYNOPSIS SRMENIA” CJSC SG  
*Protocol No. 5 of. 22.02.2005*
- At the sitting of the **Computer Systems and Informatics Department** authorities  
*Protocol No. 4 of. 28.02.2005*

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## INTRODUCTION

Course program on “**VLSI Design Algorithms**” is assigned for undergraduate education on “**Electronic Design Automation**” specialization and is taught on the 7<sup>th</sup> semesters (4 year’s 1<sup>st</sup> semester).

The course duration is 60 hours, lectures volume is 45 hours and practice classes are 15 hours.

## COURSE GOALS AND OBJECTIVES

**The goal of the course is** to teach the VLSI design automation. Methods and algorithms.

**The main objectives of the course are:**

Studying algorithms of high-level and logic synthesis, floorplanning, placement and partitioning, routing and layout compaction.

At the practice classes reception of practical skills in the VLSI design automation algorithms analysis and synthesis.

**SYLLABUS**

## 1. LECTURES (45 hours)

**1.1. Introduction (2 hours).**

The VLSI design problem. The design domains. Design action. Design methods and technology.

**1.2. General-purpose methods for combinatorial optimization (6 hours).**

The unit-size placement problem. Backtracking and branch-and-bound. Dynamic programming. Linear programming. Integer linear programming. Local search. Simulated annealing. Genetic algorithms. A few final remarks on general-purpose methods.

**1.3. Algorithms of computing geometry (4 hours).**

Representation of geometrical information. Properties of pieces. Algorithms search of crossed pieces. Construction of a convex environment. Search of pair the nearest points.

**1.4. High-level synthesis (5 hours).**

Hardware models for high-level synthesis. Hardware for computations, data storage and interconnection. Data, control and clocks. Internal representation of the input algorithm. Simple data flow. Conditional data flow. Iterative data flow.

**1.5. Logic synthesis (5 hours)**

Introduction to combinational logic synthesis. Basic issues and terminology. Binary-decision diagram.(ROBDD) principles. Variable ordering. Applications to verification. Applications to combinatorial optimization. Two-level logic synthesis. Problem definition and analysis.

**1.6. Floorplanning (5 hours)**

Floorplanning concepts. Terminology and floorplan representation. Optimization problems in floorplanning. Shape functions and floorplan sizing.

**1.7. Placement and partitioning (6 hours)**

Circuit representation. Wire-length estimation. Types of placement problem. Placement algorithms. Constructive placement. Iterative improvement. Partitioning. The Kernigan-Lin partitioning algorithm.

**1.8. Routing (6 hours).**

Types of local routing problems. Area routing. Channel routing. Channel routing models. The vertical constraint graph. Horizontal constraints and the left-edge algorithm. Channel routing algorithms. Introduction to global routing. Standard-cell layout. Building-block layout and channel ordering. Algorithms for global routing. Problem definition and discussion. Efficient rectilinear Steiner-tree construction. Local transformations for global routing.

**1.9. Layout compaction (4 hours).**

Design rules. Symbolic layout. Applications of compaction. Informal problem formulation. Graph- theoretical formulation. Maximum-distance constraints. Algorithms for constraint-graph compaction. A Longest-path algorithm for DAGs. The Longest path in graph with cycles.

**1.10. A quick Tour of VLSI design automation tools (2 hours).**

Algorithmic and system design. Structural and logic design. Transistor-level design. Layout design. Verification methods. Design management tools.

**2. PRACTICE CLASSES (15 hours)**

- 2.1. Research of the computing geometry algorithms (2 hours).
- 2.2. Research of the high-level synthesis algorithms (2 hours).
- 2.3. Research of the logic synthesis algorithms (2 hours).
- 2.4. Research of the floorplanning algorithms (2 hours).
- 2.5. Research of the placement and partitioning algorithms. (2 hours).
- 2.6. Research of the routing algorithms (3 hours).
- 2.7. Research of the layout compaction algorithms (2 hours).

**METHODIC PROVISION OF THE COURSE**

To study the course the necessary list of references is given below.

The course program is compiled taking into account that the following courses had been studied beforehand:

- “IC Design Introduction”
- “Algorithms Theory”

Understanding of the course is the basis for the further specialized subjects destined by the educational plan of “Electronic Design Automation” specialization.

**REFERENCIES***Main*

1. Sabih H. Gerez. Algorithms for VLSI Design Automation. John Wiley & Sons, 1998.

*Additional*

2. Naveed A. Sherwani. Algorithms for VLSI Physical Design Automation. Kluwer Academic Publishers, 1999.
3. Michael John Sebastian Smith. Application-Specific Integrated Circuits, 1997.
4. Baker, R. Jacob. CMOS Circuit Design, Layout and Simulation. IEEE Press, New York, 1997.